The Engine of SOC Design

OSCI DAC 2007 Meeting - Panel:
Virtual platform and ESL IP exchange: Real world challenges and what's expected from OSCI TLM 2.0

Grant Martin

Chief Scientist, Tensilica

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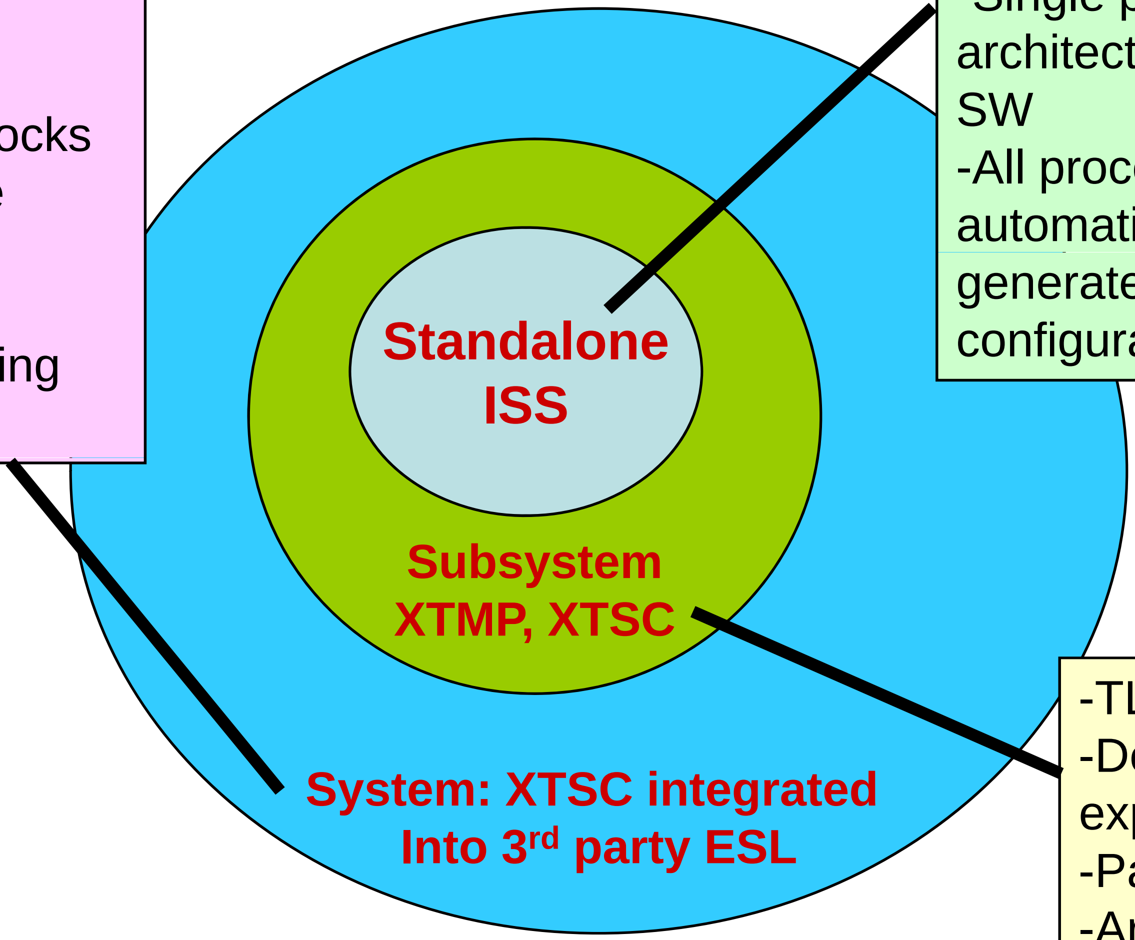
Tensilica and ESL Modelling

- Configurable, extensible processor IP
- For many years - system-level modeling with XTMP
  - C++ with a C-based API
  - Our TLM – no accepted standards
  - Cycle-accurate ISS
    - Late 2006 – fast functional mode (up to 100X)
- Late 2006 - SystemC modeling environment, XTSC
- Many interfaces
  - PIF – bus-type, memory-mapped
  - 7 local memory interfaces
  - Nearly unlimited TIE port, queue and lookup interfaces
- Interface XTSC to commercial 3rd party SystemC-based ESL tools
  - Generate adaptors: TLM_{us} to TLM_{them}
  - All TLMs different
  - Fast Functional ISS - “Virtual System Prototype” modeling

Tensilica ESL models



Standalone ISS

Subsystem XTMP, XTSC

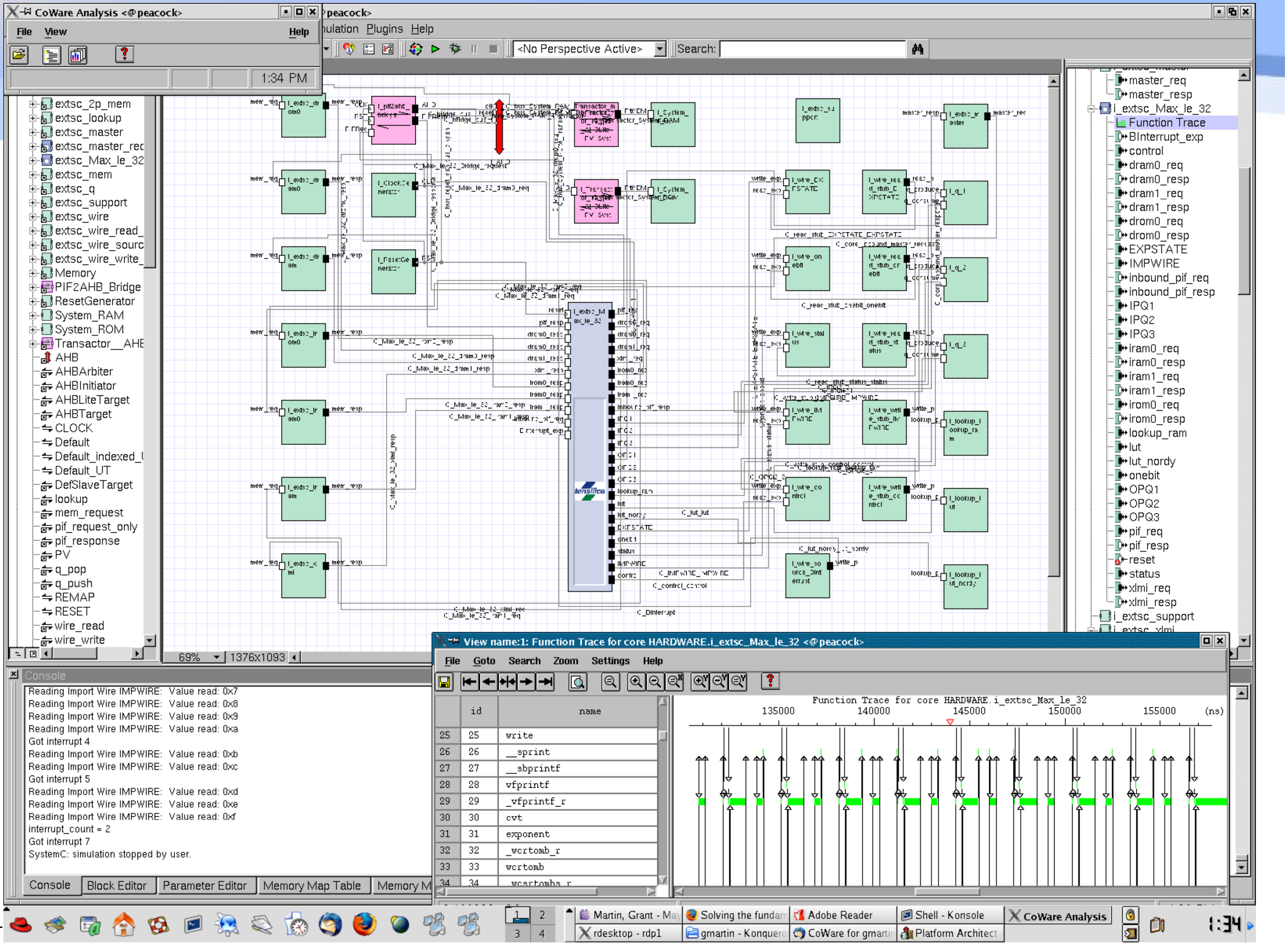
System: XTSC integrated Into 3rd party ESL

ISS
-Cycle-accurate
-Fast functional
-Single processor architect and develop SW
-All processor models automatically generated from configuration

-Complete System Model
-Buses, 3rd party processors, IP blocks
– Verify complete system at cycle-accurate level
- Develop SW using “Virtual Platform”

-TLM approach
-Design space exploration:
-Partition into MP
-Architect MP
-XTSC SystemC

Integration into 3^{rd} party SystemC-based ESL tool



```
Reading Import Wire IMPWIRE:  Value read: 0x7
Reading Import Wire IMPWIRE:  Value read: 0x8
Reading Import Wire IMPWIRE:  Value read: 0x9
Reading Import Wire IMPWIRE:  Value read: 0xa
Got interrupt 4
Reading Import Wire IMPWIRE:  Value read: 0xb
Reading Import Wire IMPWIRE:  Value read: 0xc
Got interrupt 5
Reading Import Wire IMPWIRE:  Value read: 0xd
Reading Import Wire IMPWIRE:  Value read: 0xe
Reading Import Wire IMPWIRE:  Value read: 0xf
interrupt_count = 2
Got interrupt 7
SystemC: simulation stopped by user.
```

	id	name
25	25	write
26	26	__sprint
27	27	__sbprintf
28	28	vfprintf
29	29	_vfprintf_r
30	30	cvt
31	31	exponent
32	32	_wcrtomb_r
33	33	wcrtomb
34	34	_wcsrtombs_r

TLM Evolution……..TLM 2.0

- Concerns:
  - – Too late?
    - Ad hoc integrations into 3rd party ESL tools already done
    - Little incentive to rework
  - – Priorities: For us, cycle-accurate much more important than PV+T
  - – PV+T prone to misunderstanding especially by SW developers
- Expectations:
  - – Final TLM2 needs to help industry close current gaps in interoperability
  - – Cycle-accurate - major importance
  - – Well-defined ***analysis*** and ***debug*** interfaces
  - – OSCI TLM group needs to educate users on abstractions
    - Possibly support research on PV+T estimators and system modeling
  - – Scope of TLM needs to be better defined
    - Many people assume “interoperable” TLM implies interoperable ***bus*** model implementations