SystemVerilog – Introduction & Interoperability with SystemC

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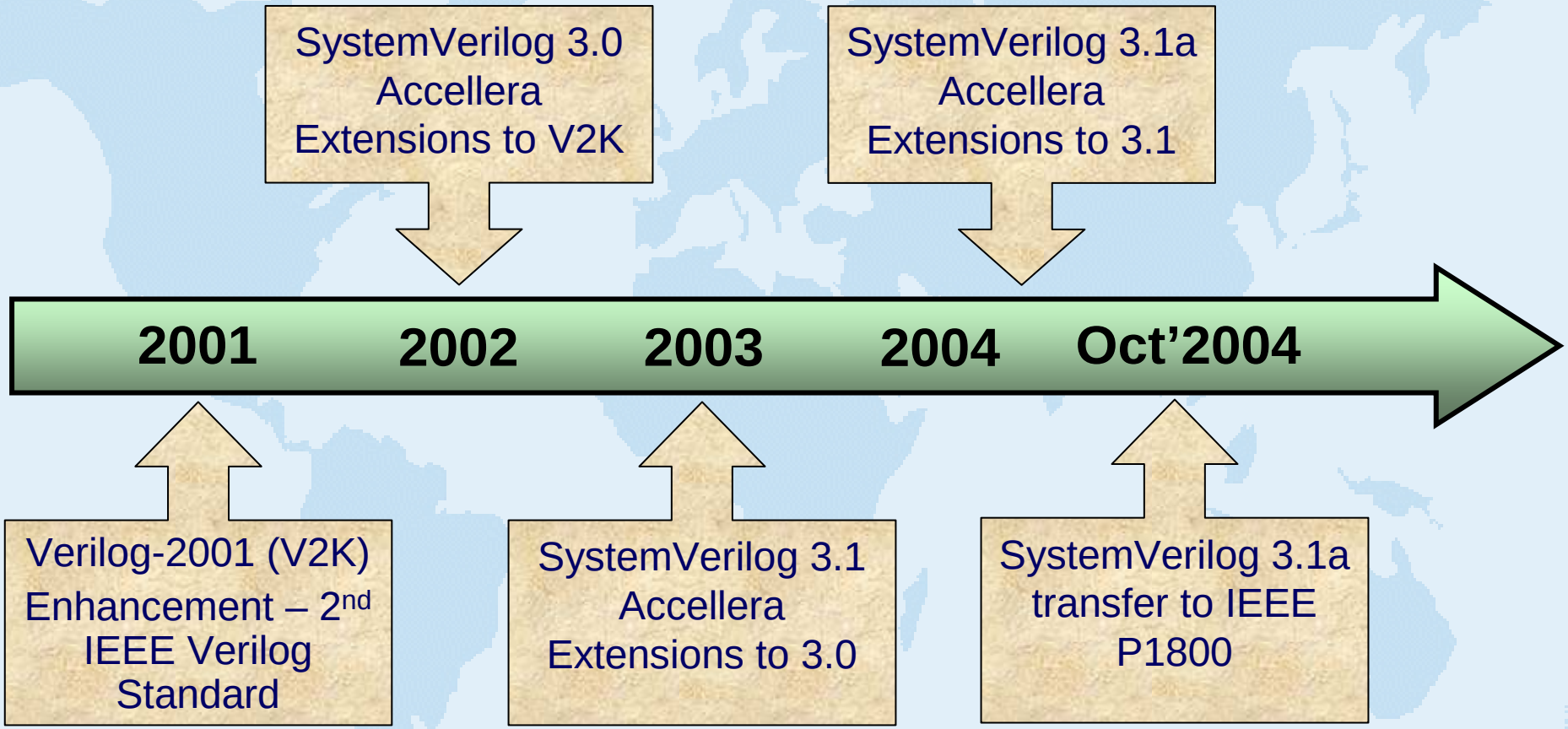
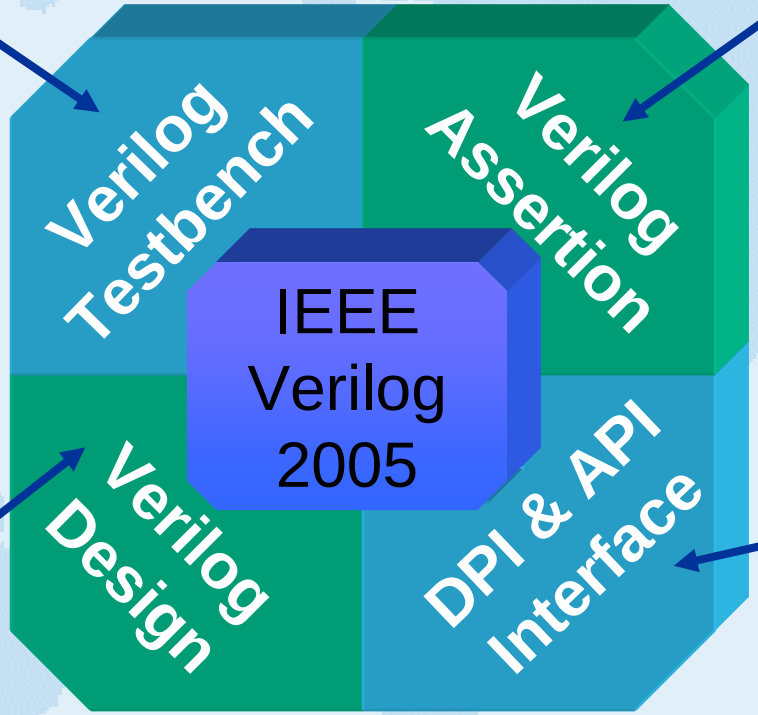
SystemVerilog History



SystemVerilog IEEE 1800 Standard was Approved in November 2005

SystemVerilog Components

Transaction-Level Full Testbench Language with Coverage



Advanced verification capability for semiformal and formal methods. The Assertion Language Standard for Verilog

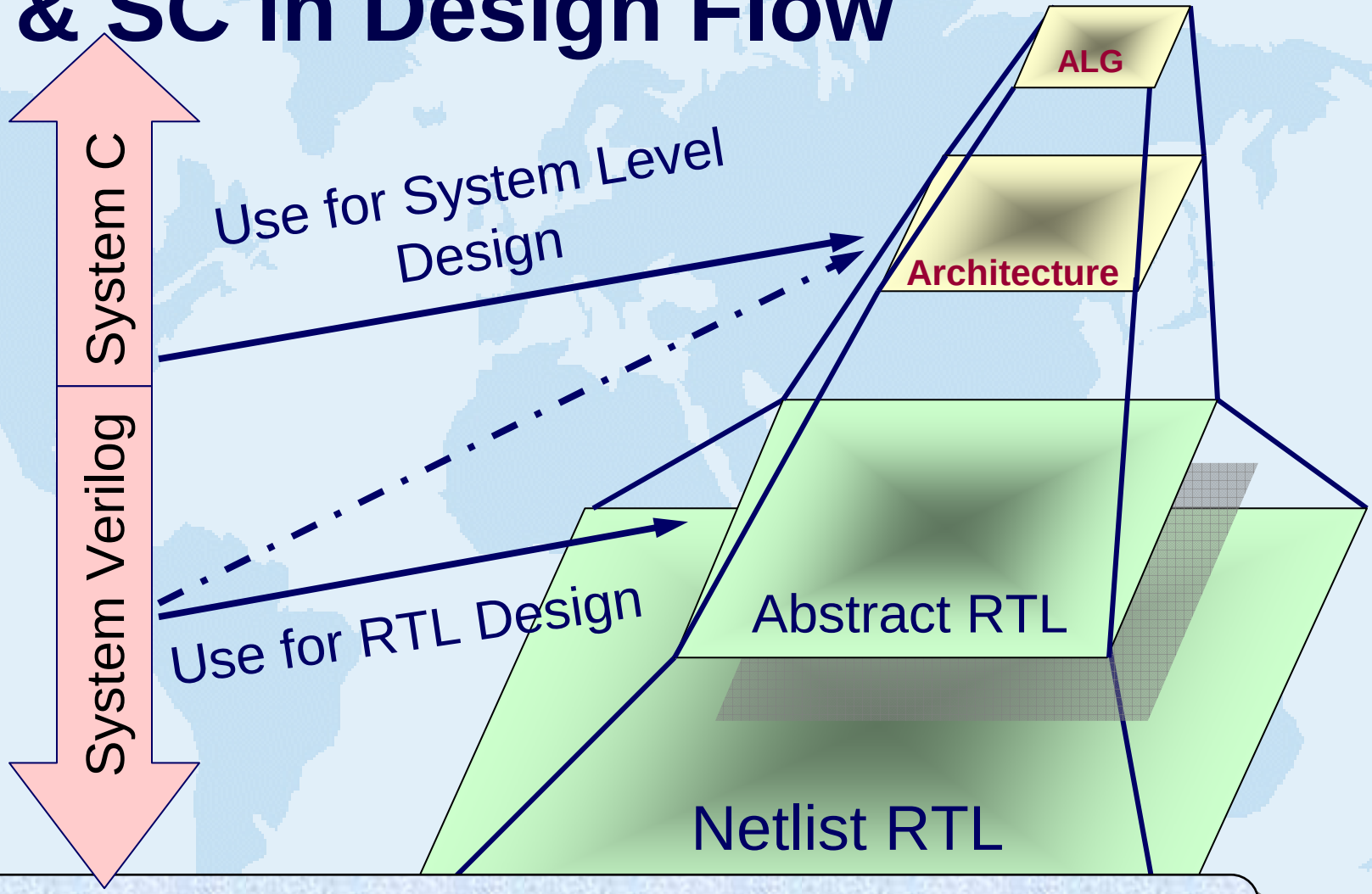
Design Abstraction: Interface semantics, abstract data types, abstract operators and expressions

Direct C interface, Assertion API and Coverage API

SystemVerilog Overview

- Leverages verification features: OO and unsized data types
  - Classes, queues, strings, dynamic arrays, associative arrays
  - Code functionality more abstractly as in C/C++
  - Refine design through levels of abstraction
- Enablement of verification as an integral part of the design language
  - Same language for abstract and detailed modeling of the design, Assertions and Test Bench
- Enablement of design Abstraction - high impact on productivity
- Concise capturing of designer intent
  - Better consistency between synthesis and simulation
- C language semantics and data types, communication interfaces
- Easy integration to external drivers implemented using a different language (e.g. C/C++)
- Wide usage and support by the EDA

SV & SC in Design Flow



System Verilog & SystemC Complement Each Other in ARCH → Physical Design Flow

Interoperability to SystemC

- SystemVerilog Direct Programming Interface (DPI) is a natural inter-language function call interface between SystemVerilog and C
  - The standard will allow for other foreign languages in the future
- DPI relies on C function call conventions and semantics
- On each side, the calls look and behave the same as native function calls for that language
  - On SV side, DPI calls look and behave like native SV functions
  - On C side, DPI calls look and behave like native C functions
- Enables integration of SystemC or Custom C/C++ models
  - Jumpstart design with high-level collateral
  - Jumpstart testbench development with early DUT

SystemVerilog Future - The Big Picture

- Develop, Approve and Publish a new IEEE standard of SystemVerilog in 2008
- A new PAR (Project Authorization Request)
  - Merge IEEE 1364 Verilog standard into P1800 SV Standard
  - Add clarifications and correct errata
  - Local enhancements to ensure successful use
  - Enhancements to SVA
  - Enhance interoperability with other standards
    - SystemC and AMS
  - Plan to maintain a “live” version of the LRM

SV Contacts & Participation

- IEEE 1800-2005 Standard for SystemVerilog : Unified Hardware Design, Specification and Verification Language Can be purchased from http://shop.ieee.org/ieeestore/
- IEEE meetings are open to the public
  - Everyone is welcome to attend meetings and voice their opinions
- Voting membership / balloting
  - By company, requires IEEE-SA membership
- Working Group (strong ties to Accellera):
  - Web site: http://www.eda.org/sv-ieee1800/
  - Chair: Srouji@US.IBM.com
  - Vice Chair: Shrenik.Mehta@sun.com
  - Secretary: dennisb@model.com