SystemC Community Update

OSCI Membership

- **Corporate Members**
  - ARM Ltd
  - Cadence Design Systems
  - CoWare
  - Forte Design Systems
  - Mentor Graphics
  - Philips
  - Synopsys
  - Summit Design Inc
  - ST Microelectronics

- **Associate Corporate Members**
  - Actis
  - Atrenta, Inc.
  - Bluespec
  - Calypto Design Systems
  - Carbon Design Systems
  - Celoxica Ltd
  - Chipvision Design Systems
  - Denali
  - Doulos
  - ESLX Inc.
  - Freescale
  - Fraunhofer Institute for Integrated Circuits
  - Intel Corporation
  - GreenSocs
  - Jeda Technologies
  - NEC Electronics America
  - SpiraTech Ltd.
  - Springsoft
  - Synfora Inc
  - Tenison Technology EDA Ltd
  - Vast Technologies

30 member companies total
8 new since last year

OSCI Board of Directors and Officers

- **OSCI Board Members**
  - ARM – Nizar Romdhane
  - Cadence - Stuart Swan
  - CoWare - Pat Sheridan
  - Forte - Mike Meredith
  - Mentor - Mark Glasser
  - Philips - Ralph von Vignau
  - STMicroelectronics - Alain Clouard
  - Synopsys – Marcus Willems

- **OSCI Officers**
  - Chairman, Alain Clouard
    - alain.clouard@ST.com
  - President, Mike Meredith
    - mmeredith@ForteDS.com
  - Executive Director, Pat Sheridan
    - psheridan@CoWare.com
  - Secretary, Paul Tauber (Legal counsel)
    - PJT@cpdb.com
  - Treasurer, Stan Krolikoski
    - stank@chipvision.com

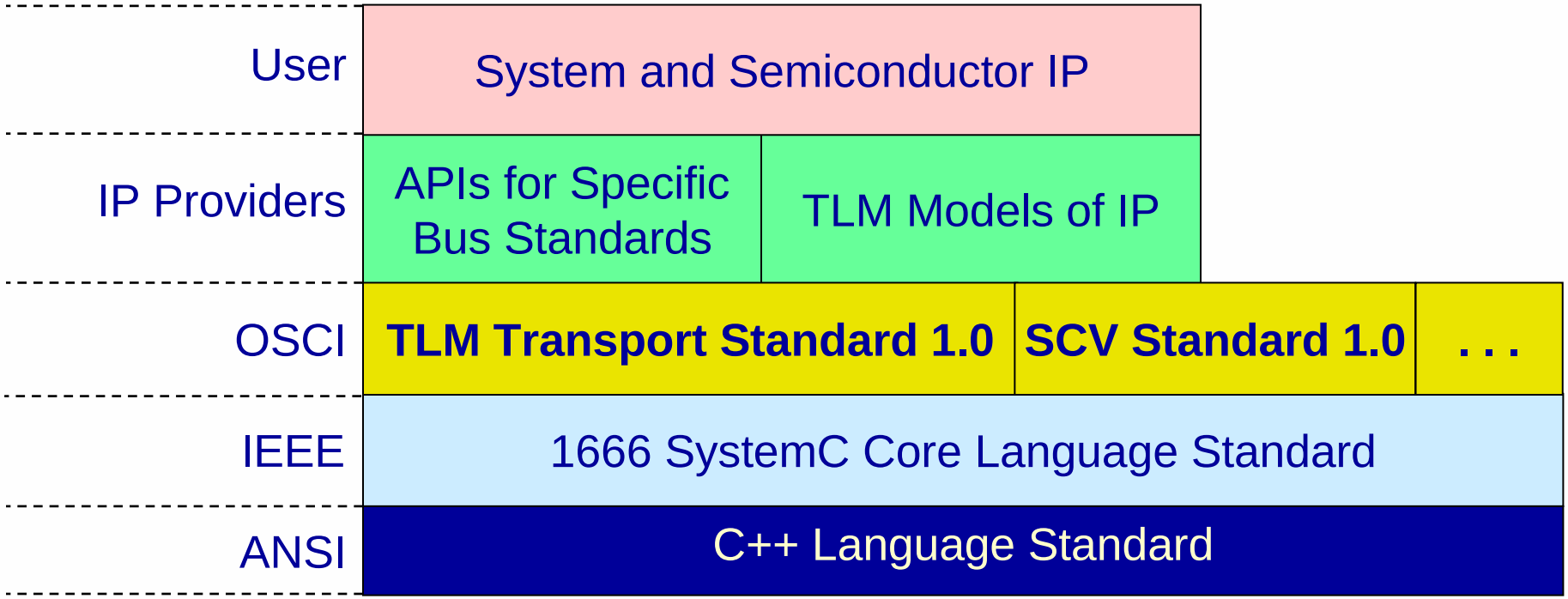
Significant OSCI Achievements This Year

- Approval of IEEE 1666™-2005 standard for SystemC
- Availability of IEEE 1666™-2005 LRM on IEEE web site without charge to users
- Release of SystemC 2.1v1 open source proof-of-concept library
- Release of SCV 1.0p2 verification library
- Public review of SystemC 2.2 library
- Public review of Synthesizable Subset document
- ~30% increase in number of member companies

SystemC Language is IEEE 1666™-2005

- Approved by IEEE on Dec. 6, 2005
- Partnership between OSCI and IEEE makes LRM available without charge to users
  - http://standards.ieee.org/getieee/1666/index.html
- Current OSCI open source proof-of-concept library 2.1v1 very close to IEEE 1666™ compatible
- OSCI library version 2.2 available in draft form for public review removes remaining known incompatibilities with IEEE 1666™-2005

SystemC Layered Standards



- **OSCI maintains open source libraries where appropriate**
  - **SystemC library**
  - **TLM library**
  - **SCV library**

TLM WG Activity

Frank Ghenassia, TLM Chair

Layered Standards

	User IP
Development Started Q305	**TLM Interoperability Layer**
OSCI : Summer 05 IEEE : 06	**TLM 1.0 – Common Transport Mechanism**
IEEE 1666	**SystemC Core Language**
ANSI C++	**C++**

Active OSCI TLM WG Members

Having an expert participating in most TLM WG conference calls :

- ARM
- Cadence
- ChipVision
- CoWare
- Doulos
- ESLX
- Forte
- GreenSocs
- Intel
- Mentor
- Philips
- SpringSoft
- ST
- Summit
- Axel Braun - Tuebingen University

- Other Organisations
  - OCP is very supportive of these efforts
    - There is significant X membership between the two organisations
    - Technical Chair of OCP is an OSCI member
  - There is also significant X membership with SPIRIT

What are we working on ?

How do we move transactions about ?

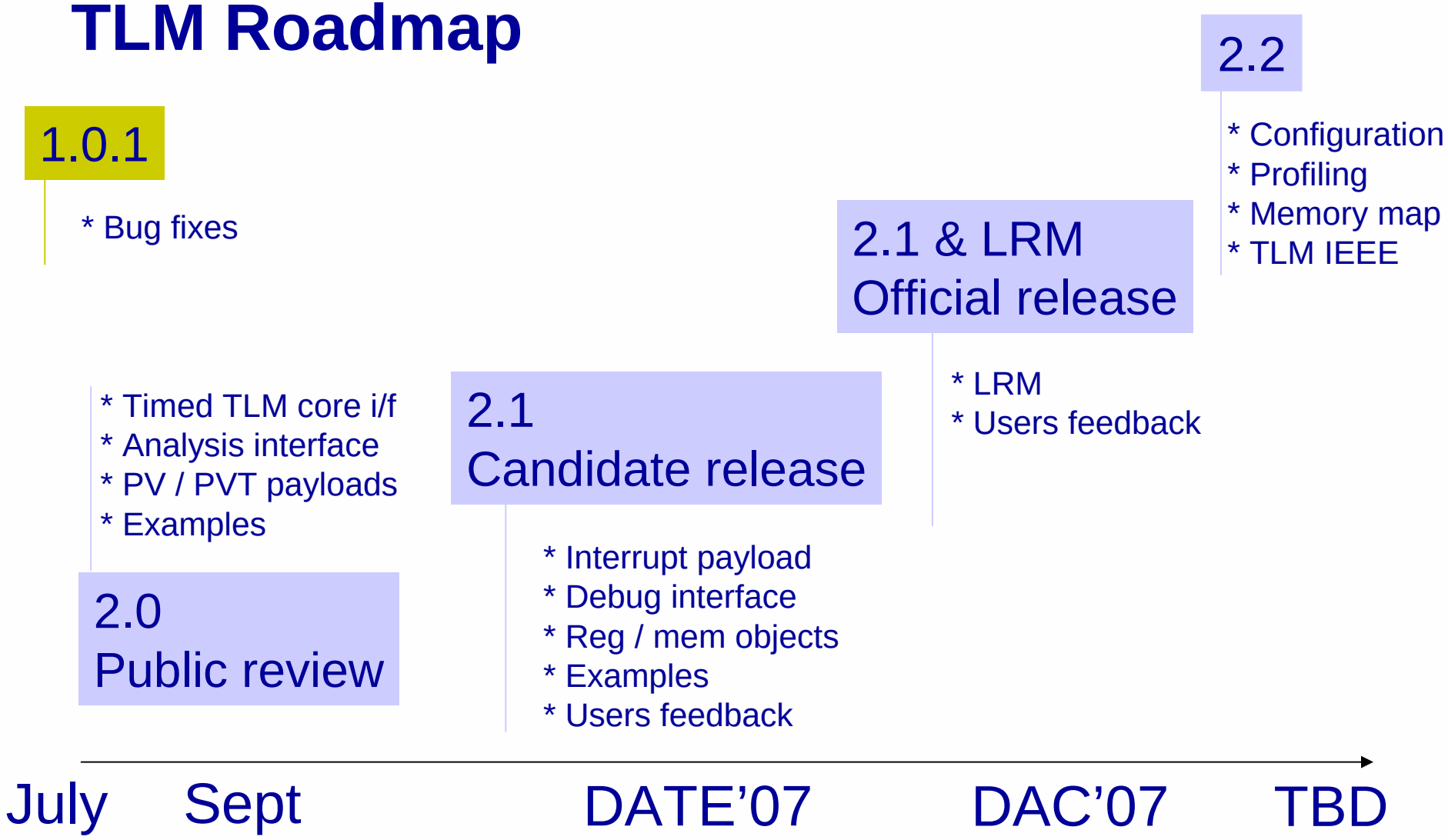
- **Minor release of existing TLM 1.0 kit (bug fixes)**
- **Standard Bus Modeling APIs**
  - **Generic PV**
  - **Generic PVT**
  - **Interrupt Modeling**
  - **Memory Map Services**
  - **Memory / Register Modeling**

What transactions do we move about ?

- **Standard Configuration and Control APIs**
  - **Configuration Interface**
  - **Debug Interface**
  - **Analysis Interface**

How do we ***control*** and ***analyse*** the transactions moving through the TLM ?

TLM Roadmap

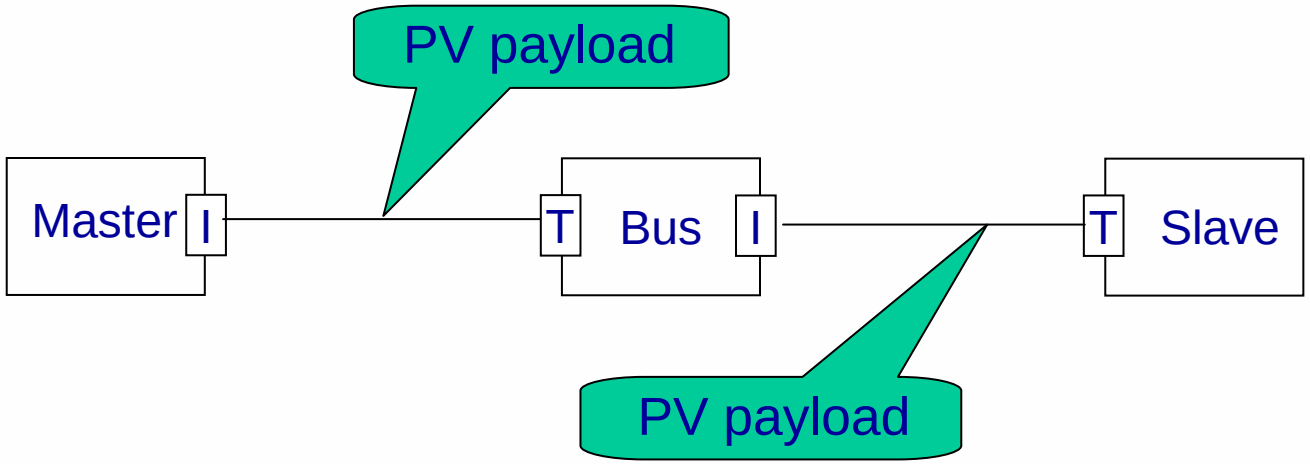

1.0.1
* Bug fixes
2.0
Public review
* Timed TLM core i/f
* Analysis interface
* PV / PVT payloads
* Examples
2.1
Candidate release
* Interrupt payload
* Debug interface
* Reg / mem objects
* Examples
* Users feedback
2.1 & LRM
Official release
* LRM
* Users feedback
2.2
* Configuration
* Profiling
* Memory map
* TLM IEEE
July
Sept
DATE'07
DAC'07
TBD

September release: Overview

- **Untimed TLM modeling**
  - **Generic PV payload**
    - **Mostly for abstract modeling of transactions over on-chip bus**
- **Timed TLM modeling**
  - **Update of core interfaces for timed modeling**
    - **Mostly sc_time parameter to core interfaces**
  - **Generic PVT payload**
    - **Mostly for performance modeling of communication over on-chip bus, taking into account pipelining**
- **Analysis interface**
  - **To monitor TLM ports**

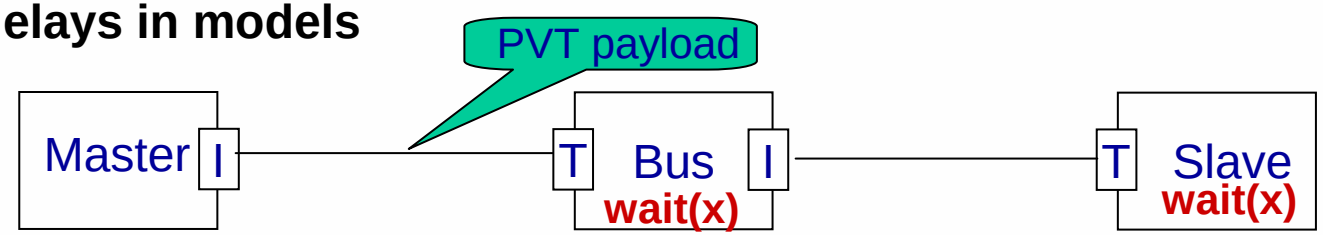
Untimed TLM modeling

- **Based on transport core TLM interface**
- **With PV payload**
- **All models using the PV payload and transport core interface can be connected and simulated together**

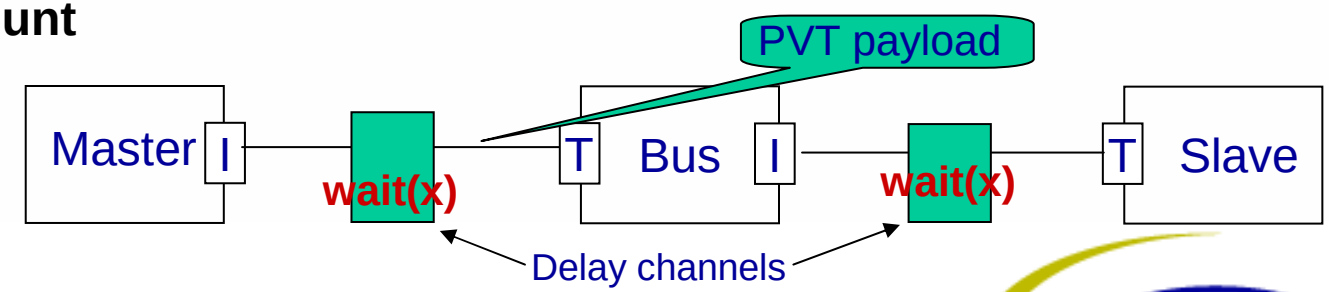


Timed TLM modeling

- **Enable timing annotations of event-based simulations**
- **With PVT payload, based on put/get core TLM interfaces**
- **All models using the PVT payload and put/get core interfaces can be connected and simulated together**
- **2 structural approaches supported:**
  - **1) Insert delays in models**



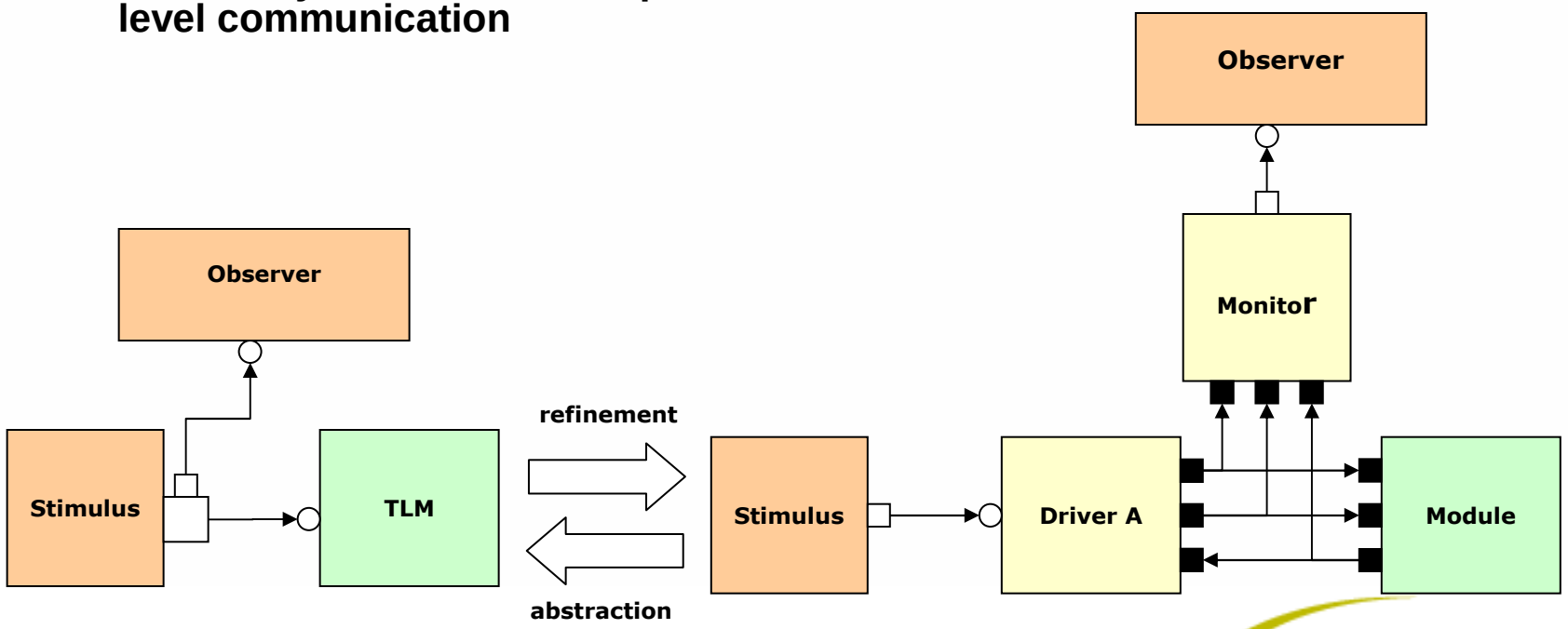
  - **2) Rely on a "delay channel" between components to take timing delays into account**



SYSTEMC™

Analysis Ports

- Non-intrusive monitoring of transactions going through TLM ports
  - Essentially, this is a SystemC implementation of the observer pattern
- Main features
  - Possibility to connect zero, one or many observers to a single analysis port
  - Non blocking interface
  - Possibility to use the same port and interface for RTL monitors and TLM level communication



Activity in Other Working Groups

Other WG activities

- Language Working Group
  - SystemC 2.2 draft available for public review
  - Repairs all known incompatibilities with 1666
- Verification Working Group
  - SCV 1.0p2 released
    - Compatible with SystemC v2.1 v1 and SystemC 2.2 (draft)
  - Work underway for future SCV releases
    - Temporal Assertion Support
      - TLM assertions
      - Signal-level assertions
- Synthesis Working Group
  - Synthesizable subset document draft available for public review
- AMS Working Group
  - Newly formed
  - Defining Analog/Mixed-signal extensions for SystemC
- Modeling Working Group
  - Proposed for creation
  - Focus on development of library of generic architectural elements based on OSCI TLM standards
  - This work is currently part of the TLM WG activity

THANK YOU