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FH Mesh_2D
Reference Manual

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Contents

1 REVISION HISTORY

Table 1

Revision	Author	Date	Description
1.00	Lasse Lehtonen	8.8.2011	Initial documentation

2 DOCUMENT OVERVIEW

2.1 SCOPE

This documentation describes the basic operation and usage of FH Mesh_2D Network-on-Chip component.

2.2 AUDIENCE

For hardware integrators wanting to use this component.

2.3 RELATED DOCUMENTATION

Table 2

Document	Description

2.4 DOCUMENT CONVENTIONS

- Ports: `teletype` in text
- Generics: `teletype` in text

3 INTRODUCTION

3.1 BRIEF DESCRIPTION

FH Mesh_2D Network-on-Chip is a highly configurable network based on 2-dimensional mesh architecture. Network can be configured to use either store-and-forward of wormhole switching, but is limited to only XY routing. Fifo depths and bus widths can be freely set and the network supports different synchronous frequencies for agents than the network's operating frequency.

3.2 EXAMPLE SYSTEM

Example system in figure 1 presents a 5 by 4 mesh topology. Every router is connected to one agent and all neighboring routers in cardinal directions with bi-directional links.

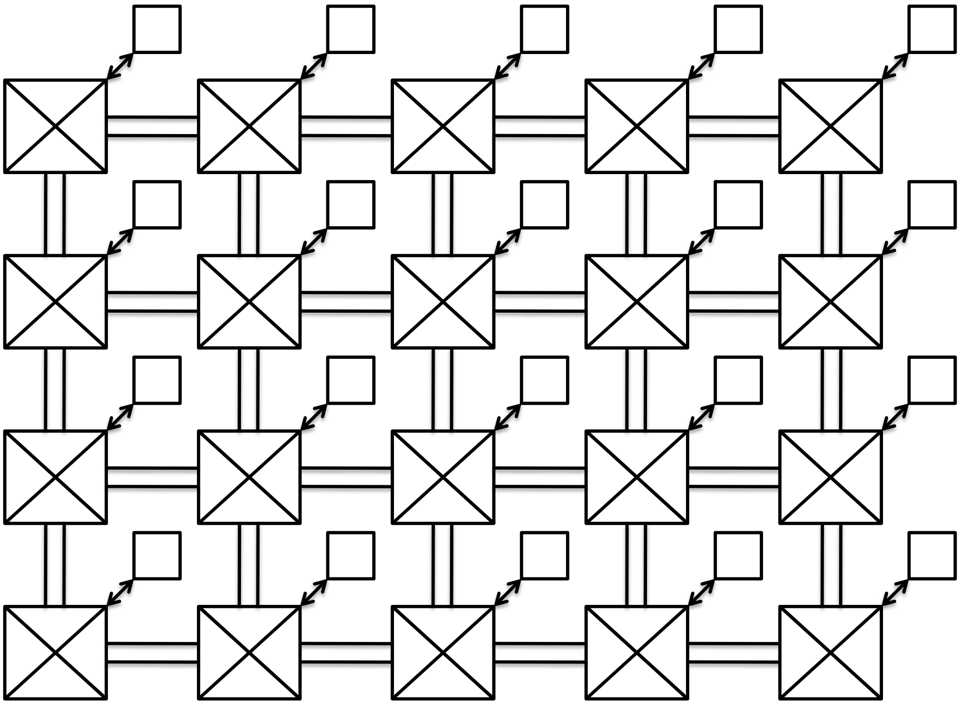

Figure 1

4 HARDWARE DESIGN

4.1 FH MESH_2D

4.1.1 GENERICS

Table 3

Name	Description
n_ag_g	Number of agents
stfwd_en_g	Selects between store-and-forward (1) and wormhole (0) switching
data_width_g	Width of the data bus in bits
addr_width_g	Width of the address bus in bits. Must be less or equal than data_width_g
tx_len_width_g	Width of txlen bus in bits
packet_length_g	Packet's maximum length in words
timeout_g	How many clock cycles to wait for packet to fill before filling it with dummy data
lut_en_g	Enable address translation
fifo_depth_g	Depth of FIFOs in words
len_flit_en_g	Enable packet to carry length information in its own flit
oaddr_flit_en_g	Enable packet to carry the destination memory-mapped address
mesh_freq_g	Network's frequency relative to IP frequecy
ip_freq_g	Agent's relative frequency to network frequecy
rows_g	Number of rows in the network
cols_g	Number of columns in the network

4.1.2 CLOCKING AND RESET

Table 4

Port	Width	Direction	Description
clk_mesh	1	in	Clock for the network, active on rising edge
clk_ip	1	in	Clock for the IP, active on rising edge
rst_n	1	in	Reset, asynchronous, active low

Clock frequencies must be at integer ratio (e.g. 1:3 but not 2:3) and they must have a synchronized rising edge.

4.1.3 DATA INTERFACE

Table 5

Port	Width	Direction	Description
tx_data_in	rows_g*cols_g*data_width_g	in	All TX datas from IPs
tx_we_in	rows_g*cols_g	in	Write enables from all IPs
tx_txlen_in	rows_g*cols_g*tx_len_width_g	in	Transfer's length in words
rx_re_in	rows_g*cols_g	in	Read enables from all IPs
rx_data_out	rows_g*cols_g*data_width_g	out	All RX datas from the network
rx_empty_out	rows_g*cols_g	out	RX FIFO empty signals
rx_full_out	rows_g*cols_g	out	RX FIFO full signals
tx_empty_out	rows_g*cols_g	out	TX FIFO empty signals
tx_full_out	rows_g*cols_g	out	TX FIFO full signals

Routers are connected to vectors starting from $(X = 0, Y = 0)$ and continuing row by row from $X = 0$ to $X = cols\_g - 1$.

4.1.4 ARCHITECTURE

Router design contains a basic synchronous FIFO for incoming links on cardinal directions and multiclock FIFOs capable of synchronous clock domain crossing for both ways connected to the Packet

Codec. Packet codec acts as network interface for IPs handling the creation of packets and the address translation from memory mapped addresses to network addresses.

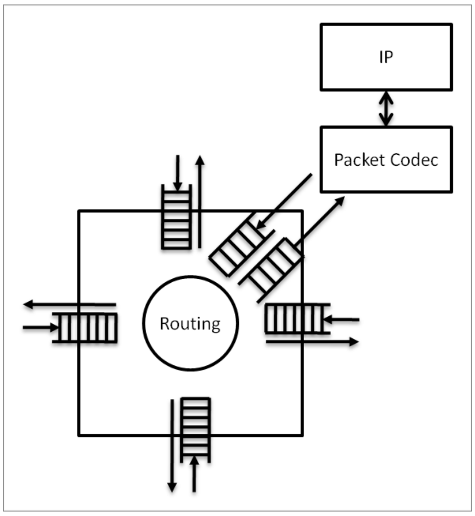

Figure 2

4.1.5 INTEGRATION

Related source files are listed in next table in the order of compilation (when applicable).

Table 6

Filename	Description
fifo.vhd	Simple synchronous FIFO
multiclk_fifo.vhd	FIFO with clock domain crossing
pkt_counter.vhd	Debug component counting packets
addr_lut_pkg.vhd	Package for pkt_codec
addr_lut.vhd	Address translation unit
pkt_enc.vhd	Packet encoder
pkt_dec.vhd	Pakcet decoder
pkt_enc_dec_1d	Top level for encoders and decoders
mesh_router.vhd	Router implementation
mesh_2d.vhd	Top level containing all routers
mesh_2d_with_pkt_codec_top.vhd	Top level with pkt_codec

4.1.6 SWITCHING

Depending on generic `stfwd_en_g` FH Mesh_2D uses either store-and-forward or wormhole switching. If store-and-forward switching is used the Packet Codec handles the creation of the network packet. If there's not enough data to fill the whole packet the unused flits will be sent empty. Packet Codec will wait few clock cycles before filling the packet to allow IP to stall a little while sending. For store-and-forward switching the FIFOs must be the same size as the packets.

For wormhole switched configuration there's no limitation to the size of the FIFOs.

4.1.7 ROUTING

Routing algorithm of FH Mesh_2D if fixed to YX-routing. Packets travel first on the Y-axis to the correct row and then along the X-axis to the destination router.

5 TESTING

5.1 TEST CASE

FH Mesh_2D network model comes with a simple test case which instantiates a 2 by 3 mesh with packet codec inteface. Test case sends one message from router (0,0) to router (1,2) and terminates after that.

5.2 SIMULATION

In order to simulate the test case one needs to compile files listed in table 6 in addition to files listed in table 7 found in basic_tester/vhd. Top level for the simulation (simple_test_mesh_2d.vhd) and the test case files are located in directory mesh_2d/sim. For the users of Modelsim also a do-file to compile needed files is supplied.

Table 7

Filename	Description
txt_util.vhd	Helper functions for printing
basic_tester_pkg.vhd	Package for Basic Tester
basic_tester_tx.vhd	Transfer generation
basic_tester_rx.vhd	Transfer validator