Transaction Generator 2 Brief

Updated: June 2, 2010

Lasse Lehtonen
Department of Computer Systems
Tampere University of Technology

1 NETWORK-ON-CHIP

Network-on-chip (NoC) term refers to a communication subsystem targeted for on chip use. Separating communication from computation allows developing on chip communication infrastructure independently from processing and other elements. Many architectures and variations of those have been developed ranging from a simple bus to a multi-hop networks with sophisticated protocols, all having different properties. For more information on network-on-chips refer to [1] and [2].

2 BENCHMARKING

As every network-on-chip topology and their individual implementations have distinctive charasteristics and thus perform differently, there is a need to benchmark NoCs to be able to choose a suitable one to use for a given system-on-chip. Development of NoCs also benefits from having common benchmarking tools to be able to easily compare if new features bring any benefits to NoC's targeted application scenarios. More about benchmarking in [3] and [4].

3 TRANSACTION GENERATOR 2

Main idea behind Transaction Generator 2 (TG), from NoC's point of view, is to create traffic according to an abstract application and platform models. TG's model of computation in its simplest form resembles Kahn process networks but can also be more versatile.

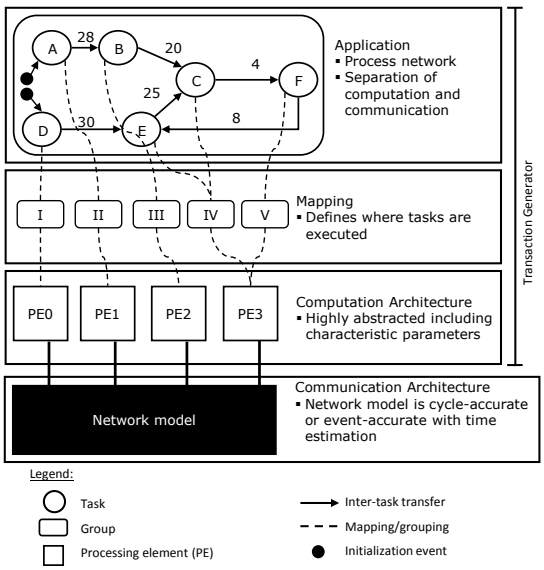

Figure 1: *Conceptual view of TG*

Transaction Generator is not an instruction set simulator (ISS) or exactly cycle accurate traffic generator but it is accurate enough for benchmarking purposes. Not being cycle accyrate makes simulation faster especially with network-on-chip models that are not cycle accurate themselves as the traffic generation will not hinder the simulation.

TG's input, the application and platform model and their mapping, is described in XML which can be easily modified by hand or generated by other programs. Transaction Generator 2 logs application model's progress and measures the utilization of the processing capabilities and the internal memories of the processing element models. It also measures individual timings from packets passed via the network-on-chip model.

Transaction Generator 2 itself is written in SystemC but it's designed to be easily used with NoC's written in other hardware description languages[1]. TG's operation does not assume any particular abstraction level from the network-on-chip model and works well with RTL and higher abstraction levels.

TG automatically collects statistics about performance, for example CPU utilization, how many times tasks have been executed, number of transferred bytes, and latency of communication. An example is shown at the snippet below.

Example application and PE measurements

```
Measuring. Current simulation time is 86 ms
* PE cpu1 utilization 0.142857 ; received    0 bytes, sent 1536 bytes,
  currently rxBuffer has  6335 bytes and txBuffer 0 bytes
* PE cpu2 utilization 0.05568  ; received 1536 bytes, sent 1152 bytes,
  currently rxBuffer has   384 bytes and txBuffer 0 bytes
* PE cpu3 utilization 0.512808 ; received    0 bytes, sent    0 bytes,
  currently rxBuffer has 21228 bytes and txBuffer 0 bytes
* PE cpu4 utilization 1        ; received 1152 bytes, sent    0 bytes,
  currently rxBuffer has 25728 bytes and txBuffer 0 bytes
* Task PreProcessing    has          1 unprocessed bytes in rx buffer, state is READY
* Task MotionEst        has        384 unprocessed bytes in rx buffer, state is RUN
* Task dct              has        384 unprocessed bytes in rx buffer, state is RUN
* Task quantization     has       1152 unprocessed bytes in rx buffer, state is READY
* Task VLC              has      23808 unprocessed bytes in rx buffer, state is RUN
* Task VLCDecoding      has          0 unprocessed bytes in rx buffer, state is WAIT
* Task Rescaling        has          0 unprocessed bytes in rx buffer, state is WAIT
* Task IDCT             has          0 unprocessed bytes in rx buffer, state is WAIT
* Task MotionComp       has          0 unprocessed bytes in rx buffer, state is WAIT
* Task MBtoFrame        has          0 unprocessed bytes in rx buffer, state is WAIT
* Task WebClient        has          1 unprocessed bytes in rx buffer, state is READY
```

4 TRANSACTION GENERATOR 2 PACKAGE

TG's package includes source codes for the main simulator program and reference network-on-chip models as well as scripts needed to compile and run the simulations. Everything is released under the LGPL license. For more details and usage instructions refer to Transaction Generator 2 Usage documentation. The package is available currently at NocBench project's web site:
`http://www.tkt.cs.tut.fi/research/nocbench/`

[1]This of course requires a simulator software capable of mixed language simulation, for example Mentor Graphics' Modelsim.

References

[1] T. Bjerregaard and S. Mahadevan, A survey of research and practices of Network-on-chip ACM Computing Surveys, Volume 38 , Issue 1, 2006, Article No. 1.

[2] Erno Salminen, Ari Kulmala, Timo D. Hämäläinen, "Survey of Network-on-chip Proposals", white paper, OCP-IP, [online]: , April 9, 2008, 13 pages.

[3] Erno Salminen, Ari Kulmala, Timo D. Hämäläinen, "On Network-on-chip comparison", Euromicro conf. on Digital System Design, Lübeck, Germany, August 27-31, 2007, pp. 503-510.

[4] Cristian Grecu, Andrè Ivanov, Axel Jantsch, Partha Pratim Pande, Erno Salminen, Umit Ogras, Radu Marculescu, "Towards Open Network-on-Chip Benchmarks", First International Symposium on Networks-on-Chip (NOCS'07), Princeton, New Jersey, USA, May 7-9, 2007, pp. 205-205, IEEE.