OCP TRACKER

Performance Realized

Product Brief

Increase productivity and quality by rapid and deterministic analysis of your system

OCP-TRACKER is a new and unique approach to SoC performance analysis and SoC traffic management. As the complexity and scale of SoC architectures advance, analysing system performance of these architectures becomes a very time consuming and tedious task. Previous methodologies involved visual inspection of signals and clock frequencies to confirm bandwidth, latencies and overall system performance at distributed points in the system.

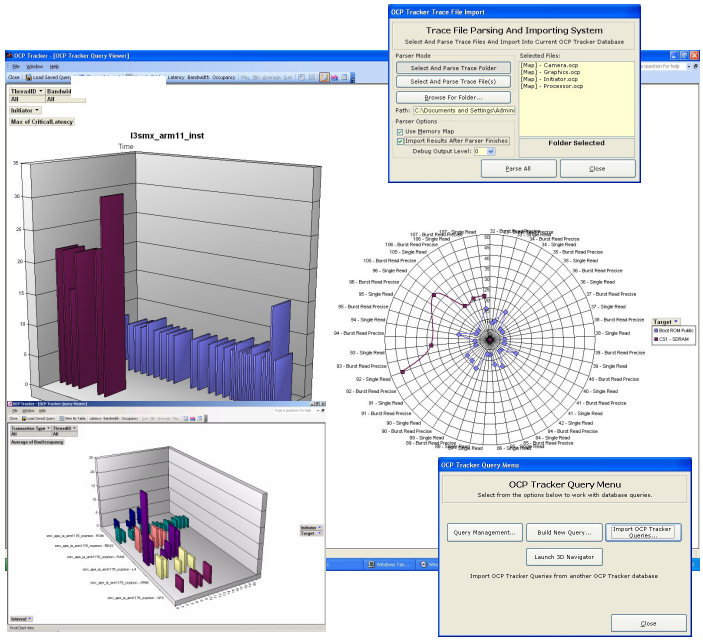
OCP (Open Core Protocol) is a standards-based, embedded-bus interface and multi-core IP integration protocol defined by the OCP-IP industry consortium.

For OCP based systems, integration and deterministic performance analysis is often a key enabler for getting products to market quickly.

Tools such as **OCP TRACKER** enable smoother system integration and deterministic performance analysis.

Highlights

- Intuitive **analysis** of complex OCP based SoC bus infrastructures
- Allows **rapid prototyping** of new SoC Architectures to determine performance criteria
- **Facilitates development** of deterministic system level performance stress testcases
- **Quickly identify** performance bottlenecks and their cause
- **Facilitates links** between SoC architecture and Design/ Validation flows and teams
- **Reduces** hard to find **critical** SoC performance bugs
- **Flexible and configurable** bandwidth and latency analysis based user-defined criteria
- Has built-in **regression manager** to manage performance based simulation environment
- **Available:** OCP 1.0, 2.0



For any OCP based SOC development OCP-TRACKER instantly enhances OCP performance analysis and debug by providing high-level information instantly to the user

TRACKER takes architectural performance analysis to the next level with the introduction of so called "intelligent analysis". This new type of analysis does not merely display waveforms of flat simulation data, but intelligently extracts the key information for the user and calculates the performance characteristics necessary, thereby accelerating system analysis. 3-D view capabilities allow more conceptual visualization of the underlying data.

With TRACKER, the performance of new architectures can be quickly analysed and the most optimum SoC architectures identified. Intelligent analysis also plays a vital role in the validation environment where the performance simulation scenarios can be qualified to ensure that the system is stressed properly. Architectural performance metrics may be migrated to the RTL/gate validation world and seamlessly inserted into a regression environment, which can be controlled by OCP-Tracker's regression manager.

Key Features

ANALYSIS

- OCP-IP transaction re-builder
- Powerful filtering engine over multiple initiators/targets
- System bandwidth, latency and bus occupancy analysis
- Max, Min latency triggering functionality – zoom to area
- 3D 360 degree free rotational visualization navigator
- 3D zoom capabilities on any bus transaction
- Comprehensive auto reports generation functionality
- Cache refill rates analysis w.r.t. system performance
- DMA request auto channel tracking analysis
- Full query building allowing customisation of analysis

SMART Monitor Features

- On-chip Smart Monitor Technology with built-in bandwidth windowing
- Supports OCP-IP version 1.0 and 2.0
- Support for SystemC and HDL OCP-IP standard trace formats
- Synthesizable smart monitor IP blocks
- Automated smart monitor integration in DV flow

Duolog Technologies—The Collaborative Design Automation Company™

Founded in 1999, Duolog Technologies, The Collaborative Design Automation™ Company, is a pioneering developer of groundbreaking EDA tools that enable the flawless and rapid integration of today's increasingly complex SoC, ASIC and FPGA designs. Duolog's Socrates Chip Integration Platform enables IC designs that are Perfect By Construction™